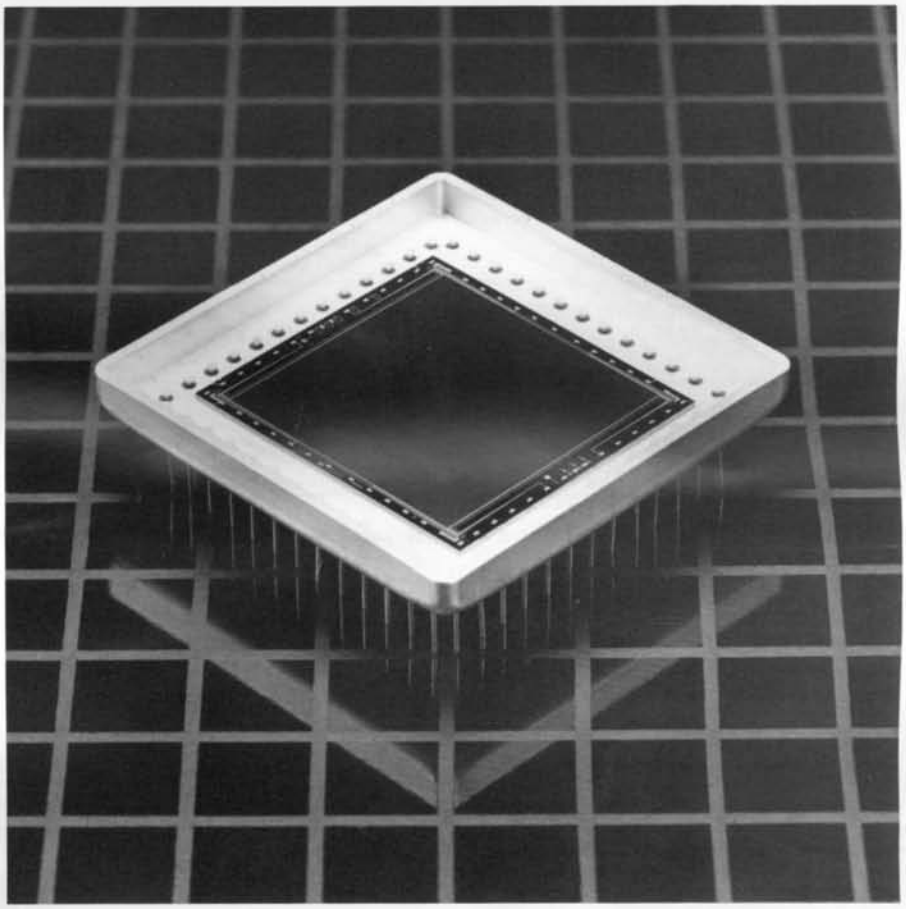
TK1024
CCD IMAGER

- Removable, protective window
- Front illumination or thinned back illumination
- Large area format: 1024 by 1024 pixels (each 24 μm square)
- Unique thinning and enhancement process:
  - Excellent QE from IR to UV
  - Antireflection coating for the visible region
  - Mechanical rigidity
- Low dark current
  - Multi-pinned-phase (MPP) technology option
- Excellent charge transfer efficiency (CTE) at low signal levels
- On-chip, low noise output transistor design for high dynamic range
- Serial-parallel-serial architecture with output MOSFETs in each quadrant to maximize readout flexibility
- Applications include astronomy, machine vision, medical imaging, X-ray imaging, and scientific imaging



General Description

The Tektronix TK1024A imager is a silicon charge-coupled device designed to efficiently image scenes at low light levels from infrared to ultraviolet wavelengths. The device is a full frame area imager fabricated utilizing a buried channel, three level poly-silicon gate process that results in extremely high charge transfer efficiency and low dark current.

This imager can be fabricated with optional multi-pinned-phase (MPP) technology, offering low dark current, minimizing surface residual image effects, and providing greater tolerance for ionizing radiation environments. MPP devices may also be operated in the non-MPP mode for larger full well capacity.

The sensor is structured in a serial-parallel-serial architecture. Low noise readout provides a convenient

Tektronix
Test and Measurement

DEVICE SPECIFICATIONS

Unless otherwise indicated, all measurements are made at standard conditions of -90 °C, 50 kpixels/second, two phases inverted, using dual slope CDS (Bandwidth = 250 kHz, at 8 μs integration time).

	Minimum	Typical	Maximum
Format		1024 by 1024 pixels full frame	
Pixel size		24 μm by 24 μm	
Imaging area		24.6 mm by 24.6 mm	
Dark current, (20 °C equiv.)			
FRONT Illum., MPP	---	0.05 nA/cm^2	0.1 nA/cm^2
" " , NON-MPP	---	0.10 nA/cm^2	1 nA/cm^2
BACK Illum., MPP	---	0.10 nA/cm^2	0.5 nA/cm^2
" " , NON-MPP	---	0.5 nA/cm^2	5 nA/cm^2
Readout noise,			
FRONT	---	5 electrons	10 electrons
BACK	---	7 electrons	10 electrons
Full well signal,			
MPP	100,000 electrons	150,000 electrons	---
NON-MPP	300,000 electrons	350,000 electrons	---
Dynamic range (relative to readout noise)			
MPP	10,000:1	20,000-30,000:1	---
NON-MPP	30,000:1	50,000-70,000:1	---
Output gain (μvolts per electron)	0.4 μV/e-	1.0 μV/e-	---
Clockline capacitance[1]			
--parallel	---	20,000 pF	---
--serial	---	600 pF	---
--transfer	---	50 pF	---
Clockline resistance[2] (parallel)			
--front illuminated, phase 1	---	90 Ω	
-- " " , phase 2	---	55 Ω	
-- " " , phase 3	---	45 Ω	
--back illuminated, phase 1	---	365 Ω	
-- " " , phase 2	---	575 Ω	
-- " " , phase 3	---	650 Ω	
-- front & back, transfer	---	60,000 Ω	
DC output level **(Limit $I_o \leq 5$ mA)**	---	18 V	---
Output data rate[3]			
--front illuminated	---	50 kpixels/s	1500 kpixels/s
--back illuminated	---	50 kpixels/s	750 kpixels/s
Output power dissipation (each MOSFET)	---	7 mW	35 mW
Charge transfer efficiency per clockcycle	.99995	.99999	---
Quantum efficiency (-90 °C)	---	(See Fig. 11 for	---
Front, λ = 400 nm	n.a.	room temp. QE)	
Front, λ = 700 nm	≥ 35 %		
Back, λ = 400 nm	≥ 35 %		
Back, λ = 700 nm	≥ 60 %		

[1]These values are obtained by integrating the current impulse necessary to charge one parallel phase [entire array] or one serial phase [entire register length], and include phase-to-phase and phase-to-substrate components.

[2]These values are obtained with PxUL/PxLL connected together and with PxUR/PxLR connected together. Resistance is measured from PxL to PxR. It includes metal bus resistance plus poly line resistance in a series/parallel combination. (Refer to Figure 3 for definitions.)

[3]The output register frequency is specified at a level where the image area clocking meets CTE specifications. Higher speeds can be achieved at lower performance levels.

Table 1: Device Specifications, TK1024A

DC OPERATING CONDITIONS

TERMINAL	ITEM	MIN	TYP	MAX	UNIT
VDDx	Output Drain Supply	15	22.5	25	V
VODx	Reset Drain Supply	10	12.3	16	V
VLGx	Feed-thru Block Gate	–5	0.5	5	V
SUB	Sub & Package Connection	–10	0	10	V
GNDx	MOSFET Ground Reference	–10	0	10	V
VOx	MOSFET Source Load	5	20	50	kohms

CLOCK VOLTAGES

TERMINAL	ITEM	MIN	TYP	MAX	P-to-P MAX	UNIT
RGx	Reset Gate				20	V
	Low Rail	–5	0	5		V
	High Rail	5	12	20		V
Sxxx	Serial Gate				20	V
	Low Rail	–10	–2	0		V
	High Rail	5	10	20		V
SWx	Summing Well				20	V
	Low Rail	–10	-1	0		V
	High Rail	5	10	20		V
Pxxx	Parallel Gate				20	V
	Low Rail	–10	–8	0		V
	High Rail	0	3	15		V
TGxx	Transfer Gate				15	V
	Low Rail	–10	–5	0		V
	High Rail	0	5	15		V
P3	High Rail*	0	6	15		V

* For MPP Devices

Table 2: DC Operating Conditions and Clock Voltages

interface to external pre-amplifiers with read-out noise typically less than 10 electrons at –90 degrees Centigrade, and 50 kpixels/second data rate. Four-quadrant architecture allows a variety of readout combinations. Tektronix' unique thinning and enhancement process, with added antireflection coating, provides increased blue and UV characteristics. The thinned die has full mechanical support, making it more rugged and easier to uniformly cool than fragile edge-supported chips. CCD imagers are mounted in a non-hermetic metal package. The packaged device is supplied with a removable, mechanically attached window to allow visual inspection and test without compromising cleanliness or protection against ESD. The device is shipped plugged into a zero insertion force (ZIF) socket which has all pins grounded to the shipping box to minimize ESD susceptibility.

Functional Description

Imaging Area

The imaging area consists of a square array of 1024 columns, each of which contains 1024 CCD picture elements (pixels). Each pixel is 24 μm X 24 μm square and the columns are isolated from each other by channel-stop regions. The device is a buried channel structure designed to take advantage of the low dark current and high CTE inherent with this process. Three levels of polysilicon are used to fabricate the three gate electrodes which form the basic CCD cell. All of the pixels in a given row are defined by the same three gates. Corresponding gates in each of the pixels in a column are bussed in parallel at both edges of the chip. The signals used to drive this section are brought in from both edges of the array, thus increasing the rate at which the columns can be clocked.

By maintaining one of the three electrical phases at a positive bias and the other two relatively low, potential wells form beneath the high gates. If an optical image is focused onto the array, an electronic analog of the scene will be collected in the potential wells.

The imaging section consists of 1025 phase 1 and phase 3 gates and 1024 phase 2 gates. (See Figure 1.) Consequently, during integration, if the phase 2 gates are held high (i.e., charge collected beneath these gates) there will be 1024 lines of data. If either phase 1 or phase 3 is held high during the integration interval, the image will consist of 1025 lines. All phase 2 parallel gates are electrically connected; phases 1 and 3 have separate electrical connections for the upper (UL/UR suffixes) and the lower (LL/LR suffixes) array halves.

Following the integration interval the device may be read out as a normal full-frame imager by transferring the collected charge one or more rows at a time into the serial (horizontal) shift register(s) and then shifting that

charge to the output. The transfer gate allows row summing into the serial register(s). It is also possible to operate in frame transfer mode, by separating the imaging array into two isolated halves.

The device is designed such that imaging data can be read out in a variety of ways. Four of the major options are represented in the CCD Timing Diagrams shown on the following pages (Figures 4,5,7, and 9).

Multi-pinned-phase (MPP) Operation

The optional multi-pinned-phase (MPP) technology available on the TK1024A allows the device to be operated totally inverted during integration and line readout. The main advantage of this mode of operation is that it results in much lower dark current than conventional CCD operation. Other advantages of MPP operation are the reduction of surface residual image effects and a greater tolerance for ionizing radiation environments.

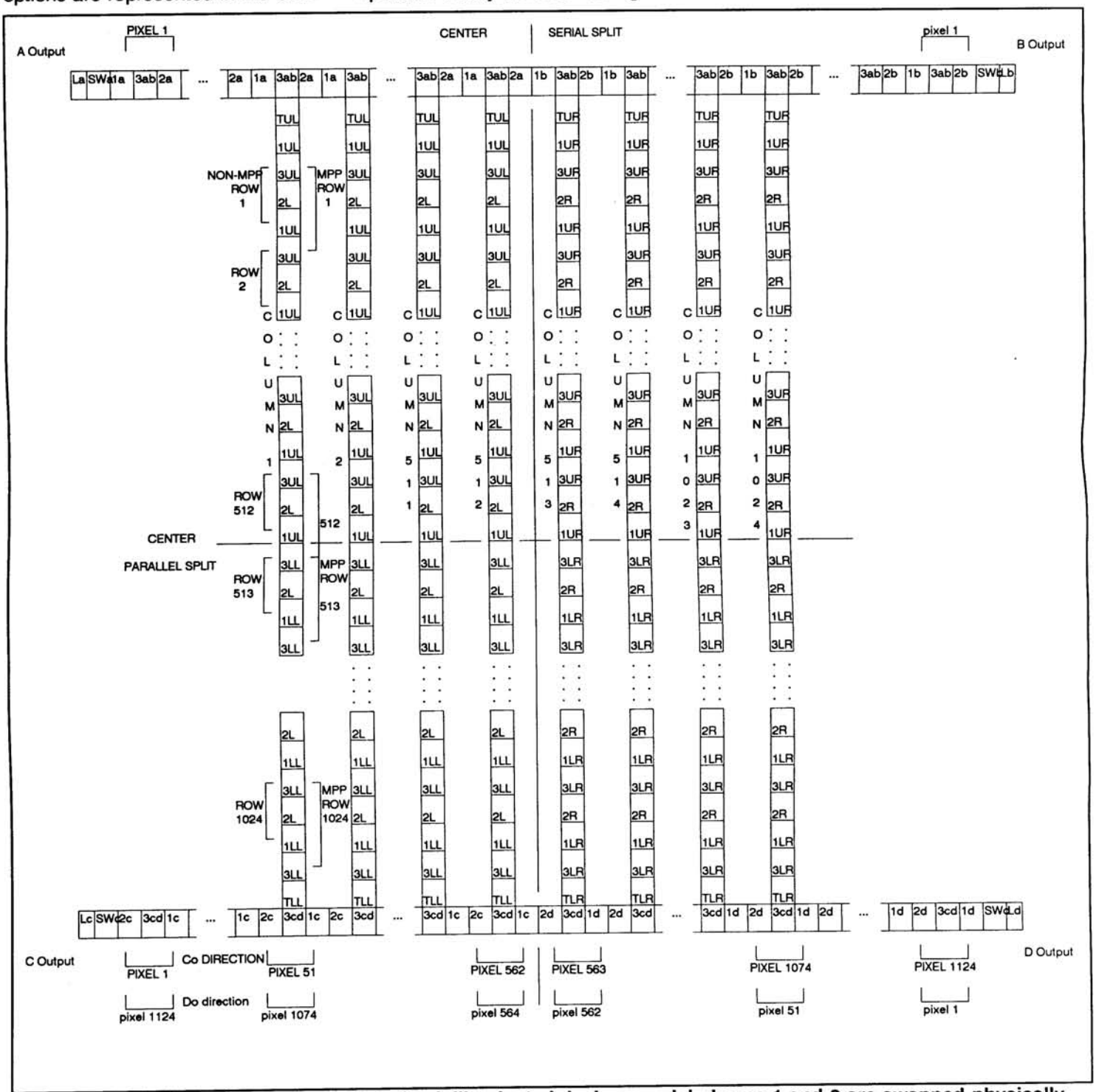


Figure 1: FUNCTIONAL DIAGRAM [For back illuminated devices, serial phases 1 and 3 are swapped physically on the device. This is accounted for in the pin definition, Table 3.]

TK1024 PIN DEFINITION

PIN #	(BACK)	FUNCTION		SYMBOL
1		Output MOSFET	Output c	VOc
2		Substrate and Package Ground		SUB
3		Reset Transistor Drain	c Register	ODc
4		Reset Gate	c Register	RGc
5		Last Gate	c Register	LGc
6	(7)	Serial Phase 2	c Register	S2c
7	(6)	Serial Phase 1	c Register	S1c
8		Serial Phase 3	cd Register	S3cd
9	(10)	Serial Phase 1	d Register	S1d
10	(9)	Serial Phase 2	d Register	S2d
11		Last Gate	d Register	LGd
12		Reset Gate	d Register	RGd
13		Reset Transistor Drain	d Register	ODd
14		Substrate and Package Ground		SUB
15		Output MOSFET	Output d	VOd
16		Output Drain Supply	d Register	VDDd
17		Output Ground Reference	d Register	GNDd
18		Summing Well	d Register	SWd
19		Transfer Gate	cd Register	TGLR
20		Parallel Phase 3	Lower Quad	P3LR
21		Parallel Phase 1	Lower Quads	P1LR
22		Parallel Phase 2	Right Common	P2R
23		Parallel Phase 1	Upper Quads	P1UR
24		Parallel Phase 3	Upper Quads	P3UR
25		Transfer Gate	ab Register	TGUR
26		Summing Well	b Register	SWb
27		Output Ground Reference	b Register	GNDb
28		Output Drain Supply	b Register	VDDb
29		Output MOSFET	Output b	VOb
30		Substrate and Package Ground		SUB
31		Reset Transistor Drain	b Register	ODb
32		Reset Gate	b Register	RGb
33		Last Gate	b Register	LGb
34	(35)	Serial Phase 2	b Register	S2b
35	(34)	Serial Phase 1	b Register	S1b
36		Serial Phase 3	ab Register	S3ab
37	(38)	Serial Phase 1	a Register	S1a
38	(37)	Serial Phase 2	a Register	S2a
39		Last Gate	a Register	LGa
40		Reset Gate	a Register	RGa
41		Reset Transistor Drain	a Register	ODa
42		Substrate and Package Ground		SUB
43		Output MOSFET	Output a	VOa
44		Output Drain Supply	a Register	VDDa
45		Output Ground Reference	a Register	GNDa
46		Summing Well	a Register	SWa
47		Transfer Gate	ab Register	TGUL
48		Parallel Phase 3	Upper Quads	P3UL
49		Parallel Phase 1	Upper Quads	P1UL
50		Parallel Phase 2	Left Common	P2L
51		Parallel Phase 1	Lower Quads	P1LL
52		Parallel Phase 3	Lower Quads	P3LL
53		Transfer Gate	cd Register	TGLL
54		Summing Well	c Register	SWc
55		Output Ground Reference	c Register	GNDc
56		Output Drain Supply	c Register	VDDc

Table 3: TK1024A Pin Definitions [The timing diagrams of Figures 4, 5, 7, and 9 are valid for front and back illuminated devices as long as the above pin nomenclature is strictly adhered to.]

To operate the CCD in the MPP mode the array clocks are biased sufficiently negative to invert the n-buried channel and "pin" the surface potential beneath each phase to substrate potential. This allows holes from the p+ channel stop to populate the surface states at the silicon/silicon oxide interface, minimizing surface dark current generation.

To enable all three phases of the array to be inverted and still retain well capacity, MPP devices have an extra implant under the phase 3 gates. During integration, this creates a potential barrier between each pixel allowing signal charge to accumulate under phase 1 and 2 at each pixel site. A consequence of this mode of operation is that the total well capacity is about 50% of that of a standard CCD, if all the parallel clocks are operated at the same voltages. A larger well capacity can be obtained if the phase 3 parallel clock is operated at higher voltages (3 to 5 volts) than the phase 1 and 2 parallel clocks.

Horizontal Registers

There are two serial (horizontal) shift registers on the chip; one at the top and one at the bottom of the imaging area. Each of these shift registers has 1124 pixels and can be further "split" in half by appropriate timing as shown in the CCD quad-output timing diagrams (Figures 7 and 9). Note that in the pin designations (as well as in timing references), these serial registers are designated as **a**, **b**, or **ab** for the top register(s); and as **c**, **d**, or **cd** for the bottom register(s). All phase 3 gates are electrically connected within each serial register: phases 1 and 2 have separate electrical connections for the left (**a**/**c** suffixes) and right (**b**/**d** suffixes) register halves.

The output of each end of the serial registers is terminated in an output summing well, a DC-biased gate (which serves to decouple the serial clock pulses from the output node), and the reset transistor. The well capacity of a pixel in the horizontal register is greater than that of a parallel pixel to ensure that CTE remains high.

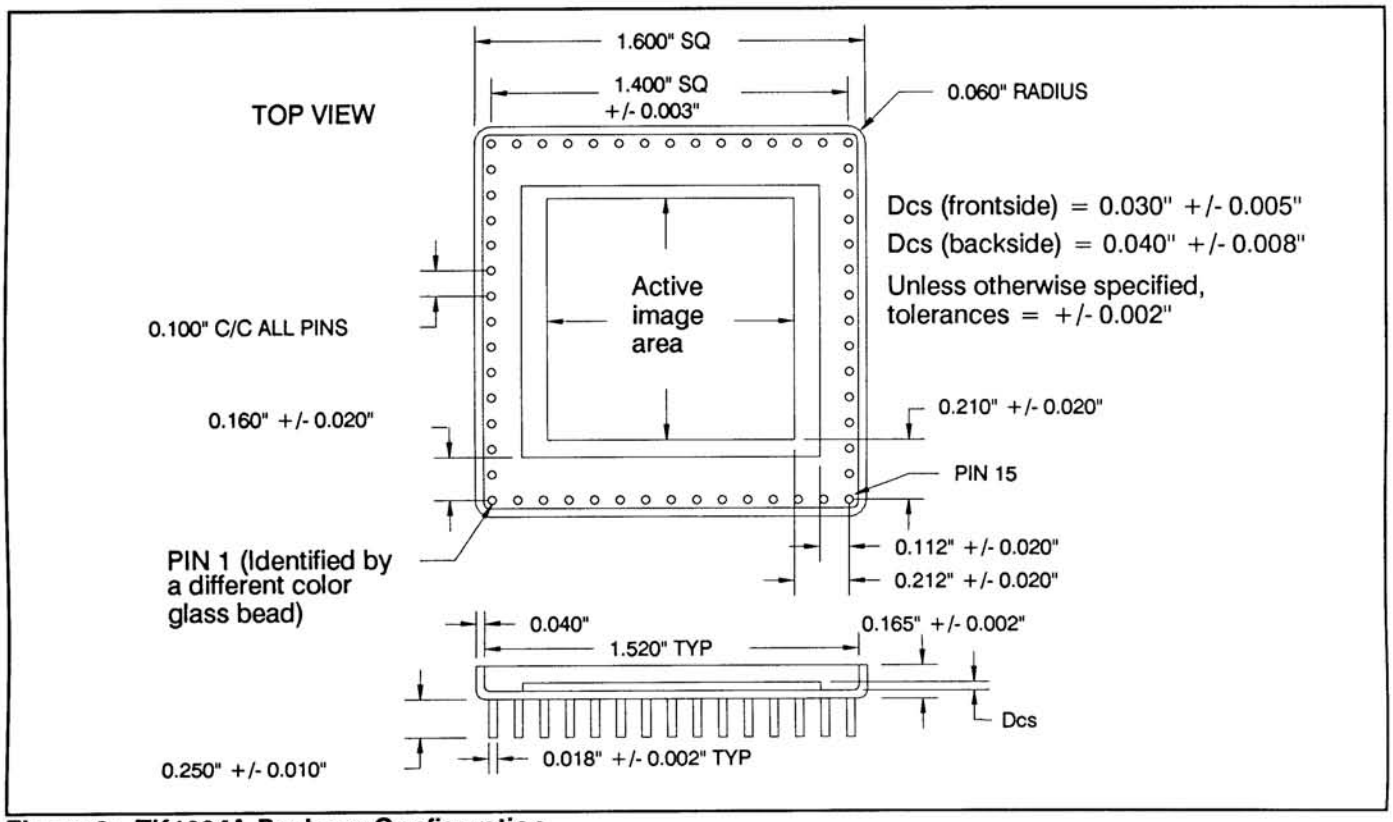


Figure 2: TK1024A Package Configuration (56 Lead Metal Package)

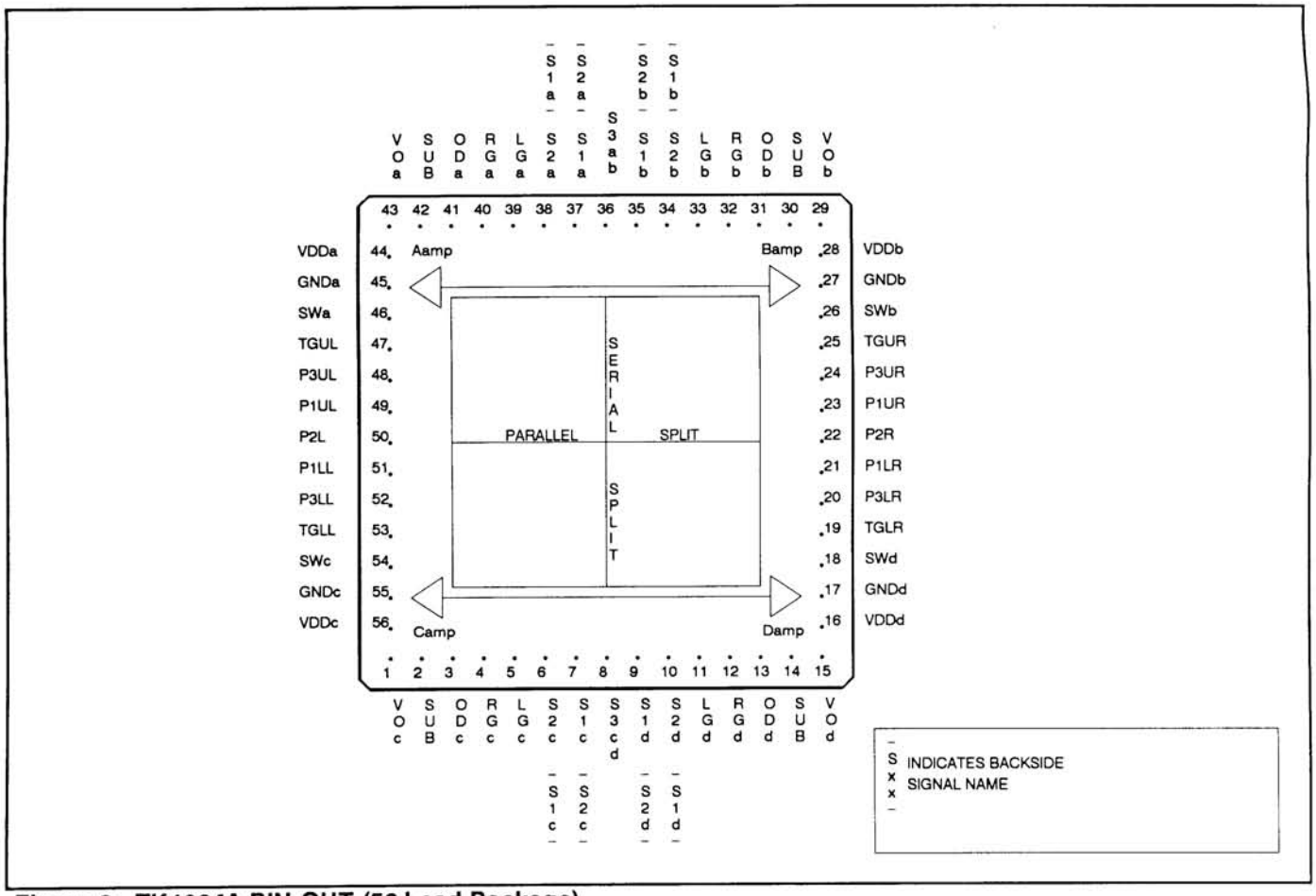


Figure 3: TK1024A PIN-OUT (56 Lead Package)

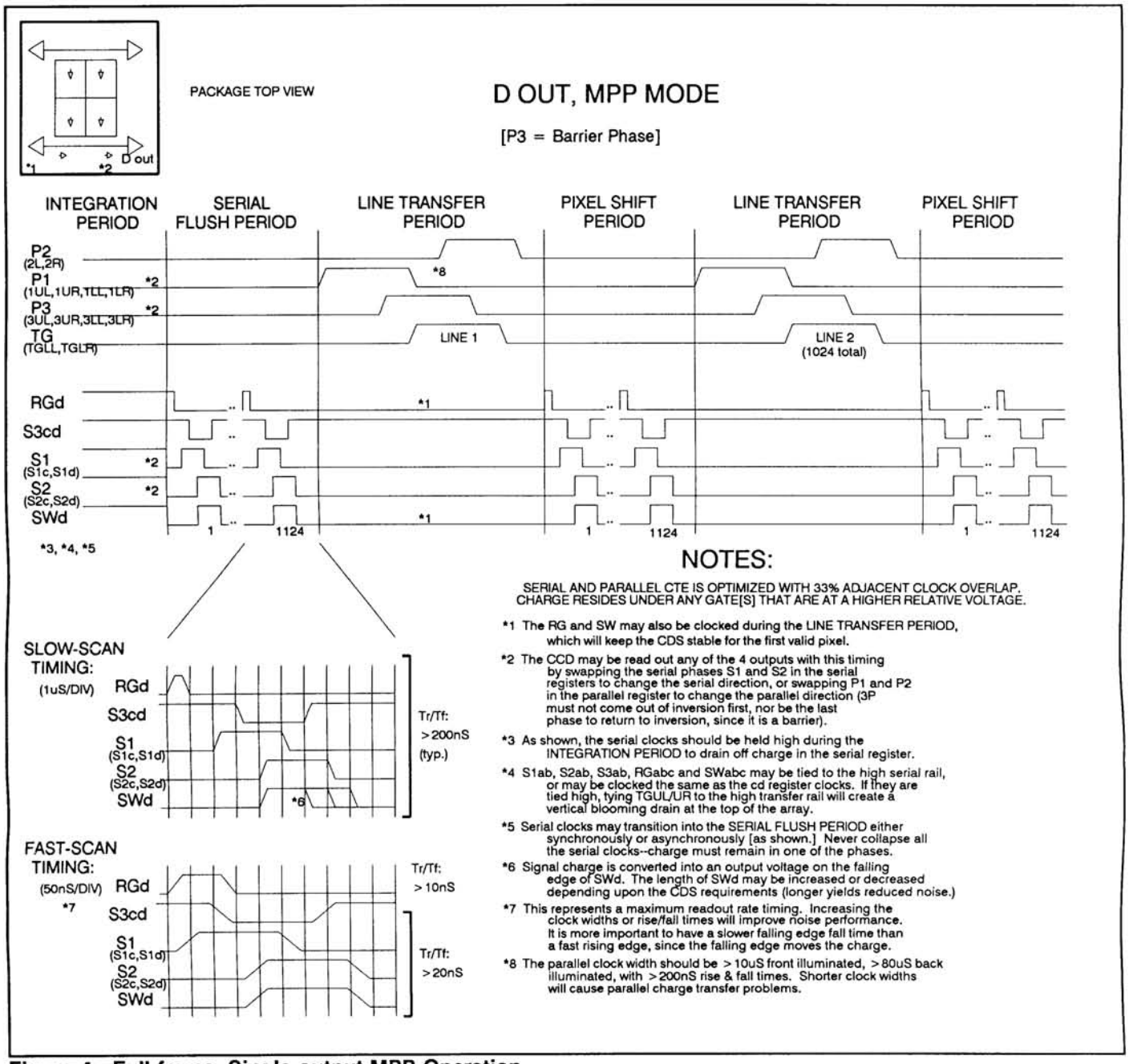


Figure 4: Full-frame, Single-output MPP Operation

Figure 1 illustrates the detailed structure of the device. The figure shows how the gates in the imaging and horizontal registers are physically related. For example, in the **cd** register, the charge collected in the imaging section can be transferred to a phase 2 gate, through the transfer gate, and then into a phase 2 gate of the serial register.

The summing well is a separately clocked gate equal in capacity to any other serial gate. Depending upon the specific application, this gate may be clocked with one of the normal serial clock phases or with its own pulse generator. The function of the summing well is to provide charge summing of consecutive serial pixels, on chip, without adding any additional noise to the process.

Using the summing well, it is possible to collect and detect the charge in small sub-arrays of the imaging section, provided that the charge sum of all pixels in the sub-array is less than the full well charge. This results in reduced array readout time and loss of resolution, but is useful where low contrast, low signal-to-noise, diffuse scenes are being imaged.

Output Transistors

The imager has four identical output MOSFETs. These are located in each corner of the device at the ends of the extended serial registers. Figure 6 presents a schematic diagram of the output configuration. All four outputs sense signals on floating diffusions.

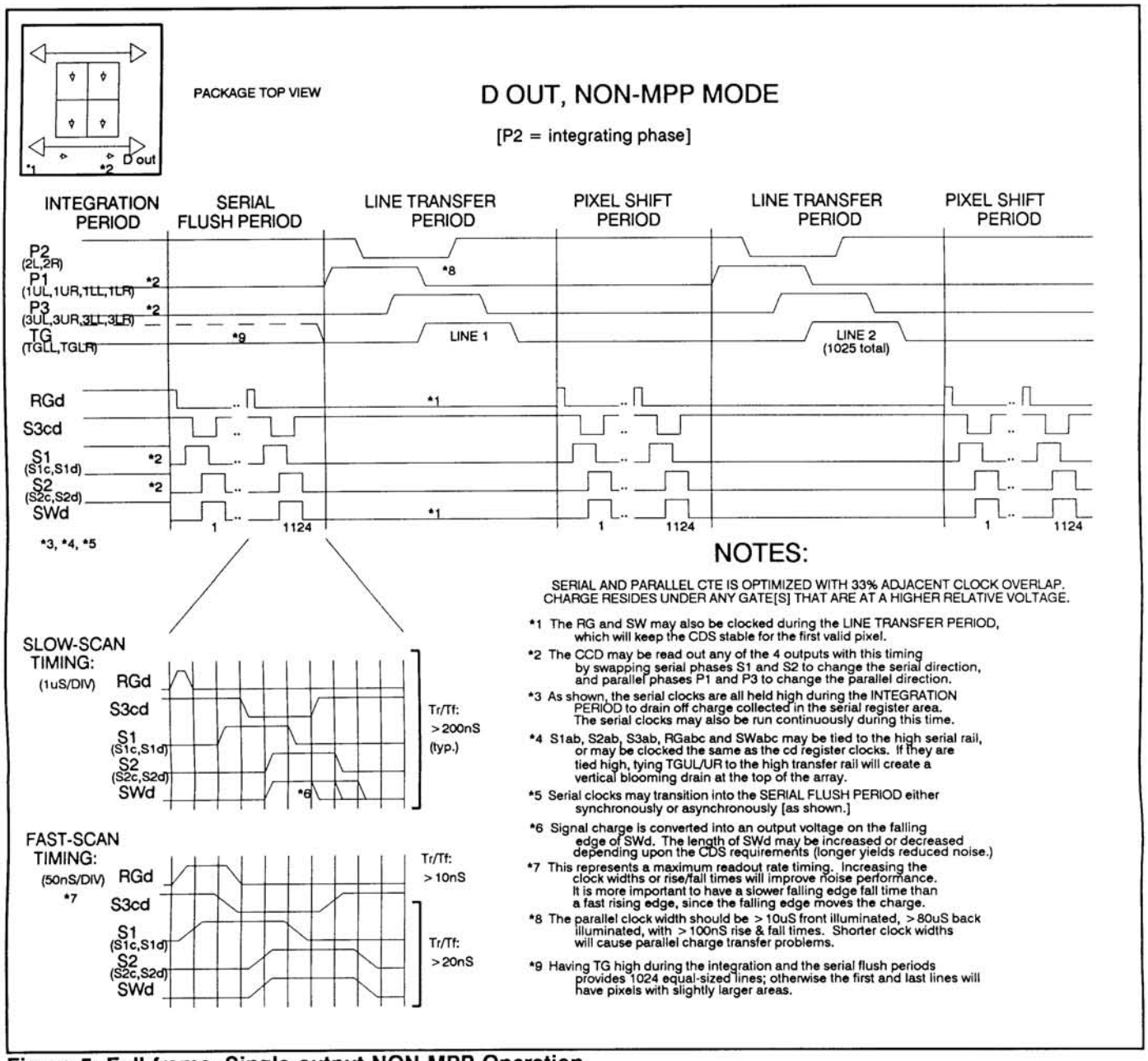


Figure 5: Full-frame, Single-output NON-MPP Operation

In normal operation, a positive pulse is applied to the reset gate. This sets the potential of the floating diffusion to the potential applied to the reset drain (VODx). The reset gate voltage is then turned off and the output node (the floating diffusion) is isolated from the rest of the circuit. Charge from a serial pixel is then collected at the output node on the falling SW edge after sequencing the serial clocks through one cycle. The addition of charge on the output node is then sensed as a change in the voltage on the gate of the output MOSFET. This change in voltage is measured at VOx.

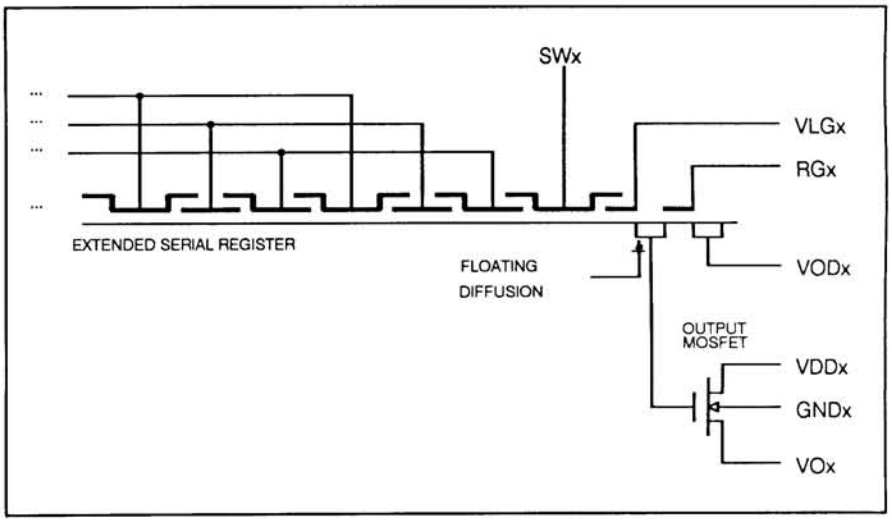


Figure 6: Output Transistor

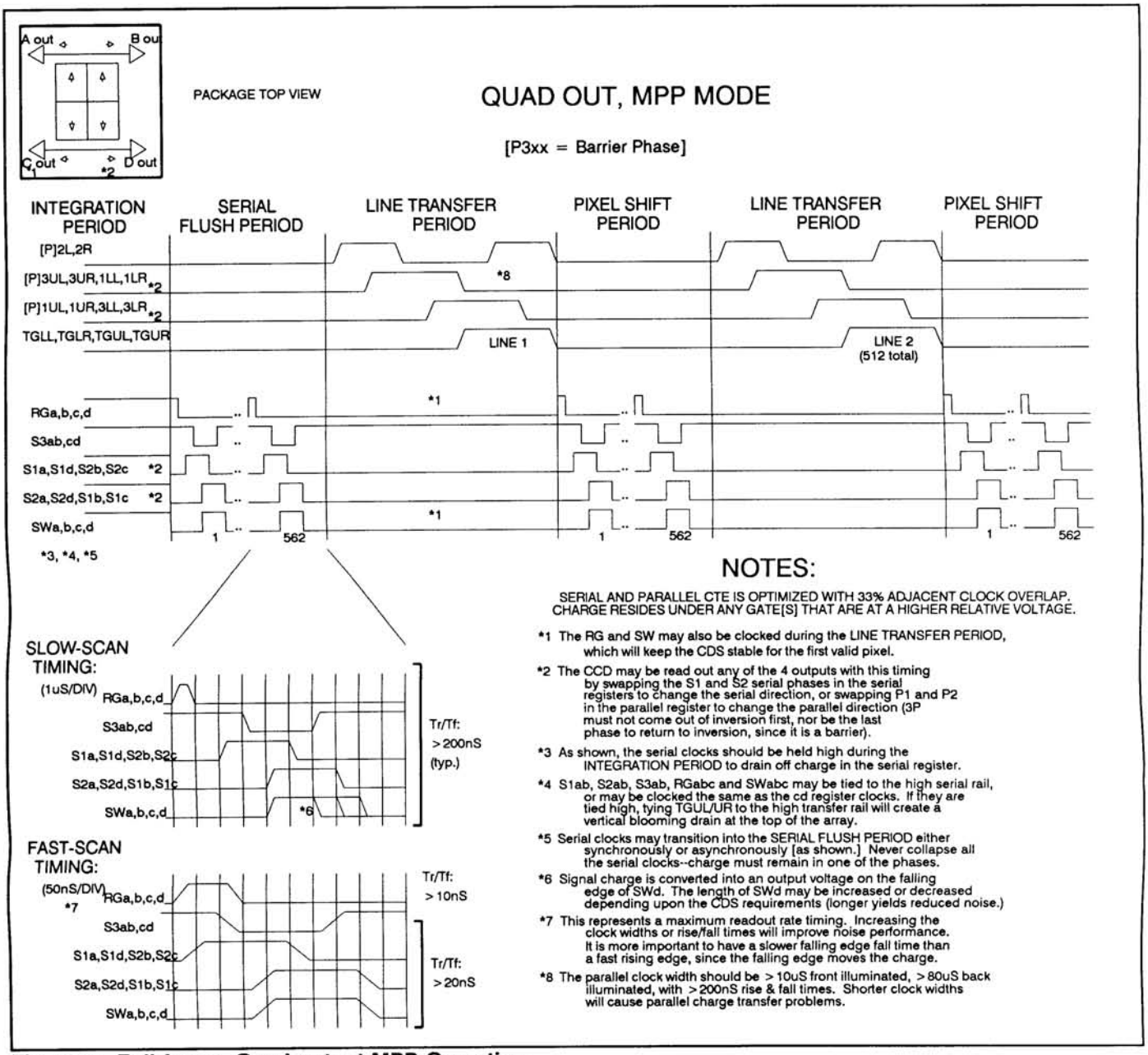


Figure 7: Full-frame, Quad-output MPP Operation

RECOMMENDED CLOCK SWITCHING PARAMETERS

	T_R and T_F MIN ALLOWED					Minimum Pulse Width				Unit
	NON-MPP		MPP			NON-MPP		MPP		
	FR	BK	FR	BK	TYPICAL	FR	BK	FR	BK	
Reset	10	20	10	20	100	100	200	100	200	ns
Serial & SW	20	40	20	40	200	200	400	200	400	ns
Parallel & TG	1	2	5	10	10	10	80	20	80	µs

NOTE: With three phase clocks, it is adviseable to have about 33% clock overlap between adjacent clock phases. (e.g. For a serial clock width of 1 µs, there should be 330 ns clock overlap.)

FR = Front-illuminated Device BK = Back-illuminated Device

Table 4: TK1024A Clock Switching

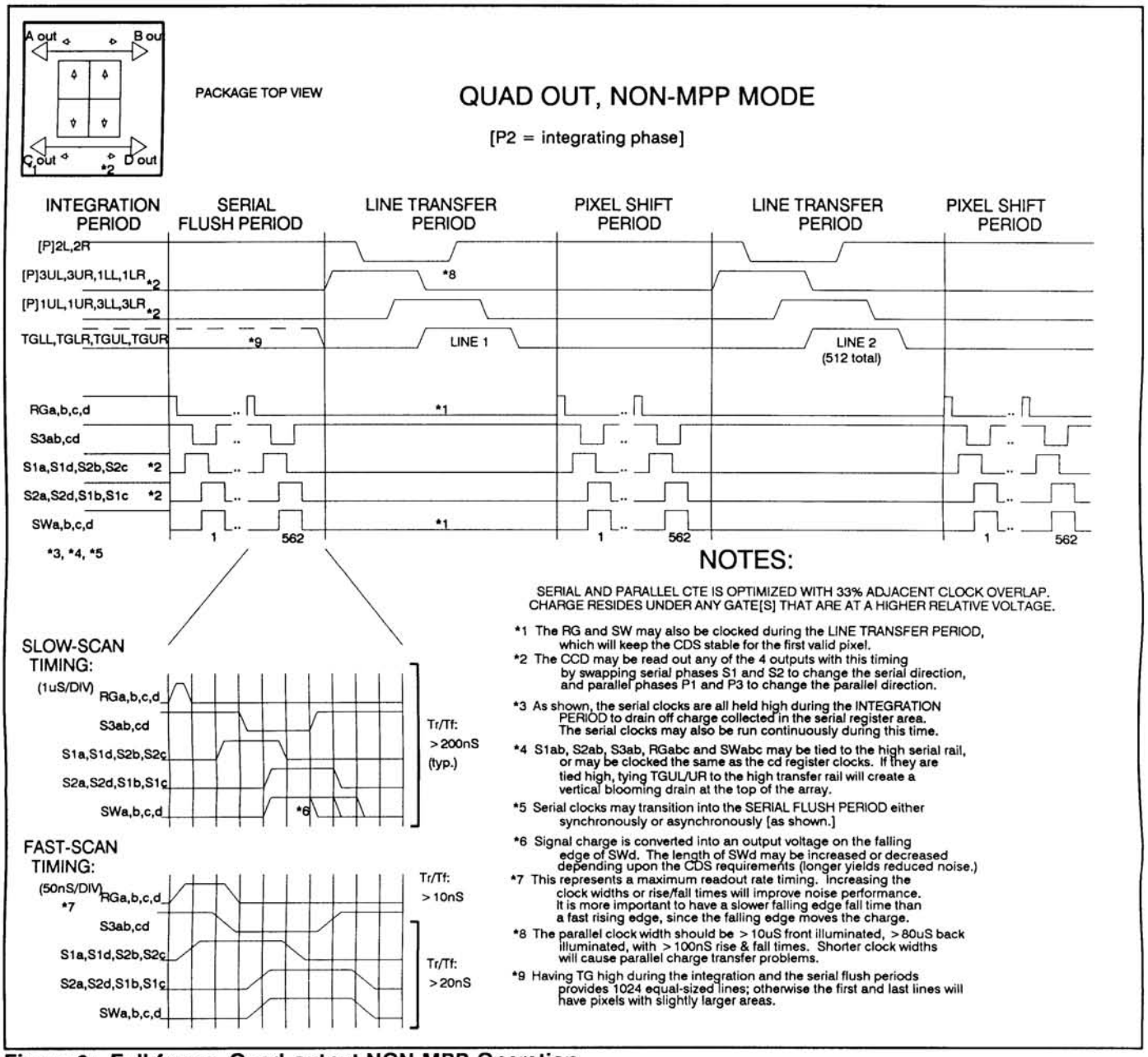


Figure 9: Full-frame, Quad-output NON-MPP Operation

Glossary

[NOTE: Defects in the outer 5 rows and columns are not measured as part of the test procedure.]

POINT DEFECT: an isolated hot pixel or dark pixel (including those caused by TRAPS), as defined below.

HOT PIXEL (DEFECT): a pixel with output 10 times higher than the maximum dark current specification when the device is integrated under dark conditions. Measured at -45 °C.

DARK PIXEL (DEFECT): a pixel with output 50% or less than the average backgound at a specific light input level. (Typically 5,000 electrons flat field signal level is used for measurement.)

CLUSTER DEFECT: two to nine contiguous defect pixels in a single column.

COLUMN DEFECT: ten or more contiguous defect pixels in a single column.

FULL WELL SIGNAL: the point where the output signal falls off 3% less than a straight line extension of the plot of output signal vs. input stimulus.

TRAP: a defect that absorbs charge as it is clocked through the defect area. Traps appear as dark defects and are counted as such.

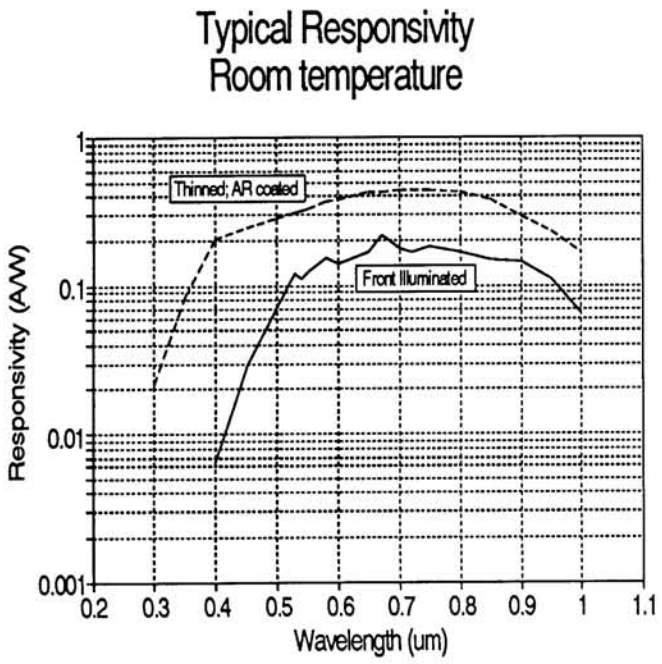


Figure 10: Typical Responsivity at Room Temperature [Top curve is for thinned, antireflection coated, back-illuminated devices. Bottom curve is for front-illuminated devices.]

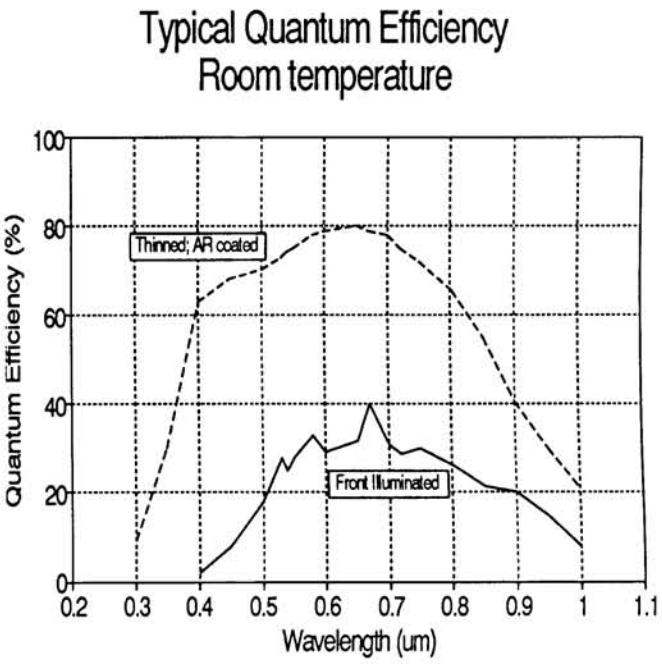


Figure 11: Typical Quantum Efficiency at Room Temperature [Top curve is for thinned, antireflection coated, back-illuminated devices. Bottom curve is for front-illuminated devices.]

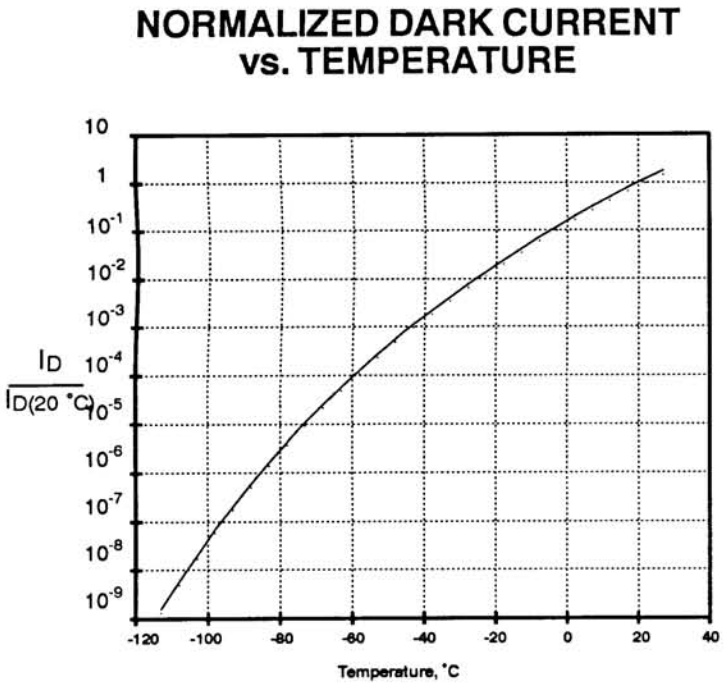


Figure 12: MPP or NON-MPP Dark Current Variation With Temperature in °C (Theoretical Data)

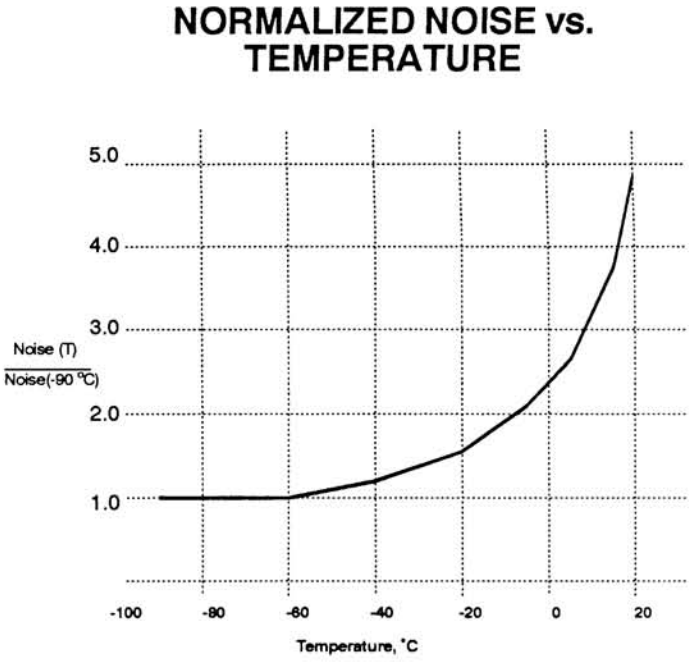


Figure 13: Output MOSFET Noise vs. Temperature in °C (excludes dark current contributions)

Product Grading

TK1024A CCD imagers are classified into several grades based upon the occurrence of pixel, cluster, and column defects and upon output characteristics. The maximum number of such defects is defined for the TOTAL ARRAY. A data sheet is shipped with each part indicating screening test results and actual operating voltages.

See the current price sheet for grading details.

Product Precautions

Input/Output

It is strongly advised that special handling precautions be taken to avoid applications of any voltage higher than the maximum rated voltage to this high impedance circuit.

For proper operation, it is recommended that all inputs, gates and outputs be constrained as indicated in Table 2 (DC Operating Conditions and Clock Voltages).

Double check the test equipment setup for the proper polarity of the voltage BEFORE conducting parametric or functional testings.

Never short the on-chip amplifier output(s) while operating.

Static Handling Procedures

All CCDs should be stored or transported in conductive material so that all exposed leads are shorted together. All TK1024A CCDs are shipped in a package with the CCD plugged into a socket which has all pins shorted to package ground. CCDs should NOT be inserted into conventional plastic "snow" or plastic trays of the type used for storage and transportation of other semiconductor devices.

All CCDs should be placed on a grounded bench surface and the operator should be grounded prior to handling the device. This is done most effectively by having the operator wear a conductive wrist strap.

Whenever handling a CCD, it is recommended that this operation be accomplished in a clean static free environment. This is particularly important for back-illuminated devices.

NOTE that without the protective window attached to the device, the bond wires are exposed and can be easily damaged.

DO NOT insert or remove CCDs from test sockets with the power applied. Check all of the power supplies to be used for testing CCDs and be certain that there are no voltage transients present.

When any lead straightening or hand soldering is necessary, provide ground straps for the apparatus used.

Cold chambers used for cooling devices should be antistatic and should not allow moisture condensation on the device.

Ordering Information

Part numbers for ordering TK1024A CCD imagers designate defect grades and number of functioning output ports.

Information contained herein represents typical device specifications, but may not reflect all possible parameters.

Consult your Tektronix Microelectronics Regional Sales Manager for further information.

[See the Tektronix regional sales map for the United States and Canada.]

International:

TEK France: Orsay Office
PHONE: 33 (1) 69-86-81-81
FAX: 33 (1) 69-07-09-37

TEK Germany: Nürnberg Office
PHONE: 49 911 34 891
FAX: 49 911 34 67 50

TEK U.K.: Marlow Office
PHONE: 44 (628) 486000
FAX: 44 (628) 474799

Microelectronics Products Line
Tektronix, Inc.
P.O. Box 500
Mail Station 59-420
Beaverton, OR 97077
PHONE: (503) 627-4869
FAX: (503) 627-5560
TLX: 151754

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Test and Measurement